

TITLE: A SILICIDED BURIED BITLINE PROCESS FOR A NON-VOLATILE MEMORY CELL INVENTOR(S): Daniel Sobek, Timothy J. Thurgate, Mark W. Randolph USSN: 09/885,426 Attorney Docket # AMD-E306

1/5 Replacement Sheet

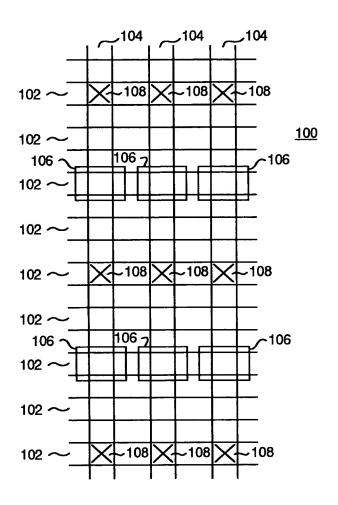


FIG. 1

PRIOR ART

USSN: 09/885,426 Attorney Docket # AMD-E306 Replacement Sheet Periphery Isolation - 202 **Periphery Well Formation** - 209 Periphery Vt Implanting - 206 Core Implanting - 208 Gate Formation **Gate Formation** Floating Gate Polysilicon 1 Deposition - 212 **Gate Patterning** - 214 **Pocket Implanting** - 216 **Etching** - 218 **Bit-Line Formation** - 220 **Spacer Deposition** - 222 **Spacer Etching** - 224 Silicidation - 226 Oxide Deposition - 228 **Planarization** 230 **ONO Formation Wordline Deposition**

FIG. 2

- 232

TITLE: A SILICIDED BURIED BITLINE PROCESS FOR A NON-VOLATILE MEMORY CELL

INVENTOR(S): Daniel Sobek, Timothy J. Thurgate, Mark W. Randolph USSN: 09/885,426 Attorney Docket # AMD-E306

3/5

Replacement Sheet

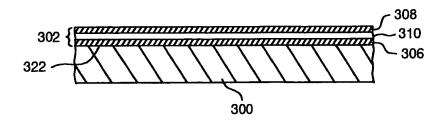


FIG. 3

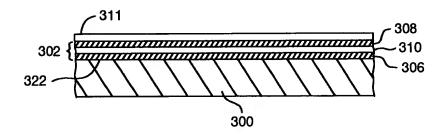


FIG. 4

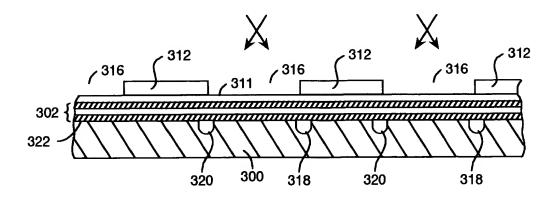


FIG. 5

TITLE: A SILICIDED BURIED BITLINE PROCESS FOR A NON-VOLATILE MEMORY CELL

INVENTOR(S): Daniel Sobek, Timothy J. Thurgate, Mark W. Randolph

USSN: 09/885,426 Attorney Docket # AMD-E306

4/5

Replacement Sheet

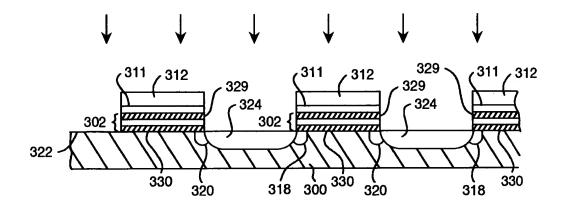


FIG. 6

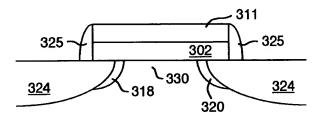


FIG. 7

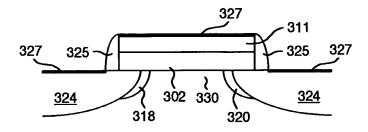


FIG. 8

TITLE: A SILICIDED BURIED BITLINE PROCESS FOR A NON-VOLATILE MEMORY CELL INVENTOR(S): Daniel Sobek, Timothy J. Thurgate, Mark W. Randolph USSN: 09/885,426 Attorney Docket # AMD-E306

5/5

Replacement Sheet

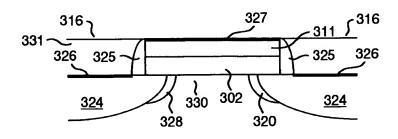


FIG. 9

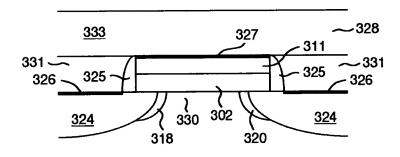


FIG. 10

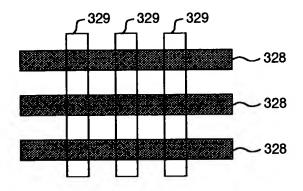


FIG. 11